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10/596,727	06/22/2006	Makoto Yasusaka	40404.41/ko	9932

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EXAMINER	
CHENG, DIANA	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
05/07/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/596,727	YASUSAKA, MAKOTO	
	Examiner	Art Unit	
	DIANA J. CHENG	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8 and 10-14* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments filed 03/18/2008 have been fully considered but they are not persuasive.

Drawings

2. The replacement drawings were received on 06/22/2006. These drawings are not acceptable due to missing a connection point for element 15. Therefore, it is not clear where the other end of 15 is connected to.

3. The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Taneji et al. ((JP 08-191238), as cited in the IDS dated 06/22/2006.

Re claim 7, Taneji et al. discloses in Fig. 5 a signal output circuit comprising:

an output transistor of an NPN type bipolar transistor arranged to output an output signal (37);

a ground side output control transistor that turns ON and OFF according to an input signal so that turning ON drops the potential of a base of the output transistor to turn OFF the output transistor, and turning OFF raises the potential of the base of the output transistor to turn ON the output transistor (35);

a base current supply resistive element arranged to supply current from an input power supply to the base of the output transistor (R7);

a power supply side output control transistor located between the base current supply resistive element and the base of the output transistor and arranged to turn ON and OFF in opposite ways as the ground side output control transistor according to the input signal (36);

a ground side current bypass transistor, that turns ON and OFF in the same way as the ground side output control transistor according to the input signal so that turning ON allows current of the base current supply resistive element to flow in order to drop the voltage applied to the power supply side output control transistor and turning OFF stops the current of the base current supply resistive element from flowing (34); and

a current limitation resistive element located between the ground side current bypass transistor and the base current supply resistive element that limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow (R6).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taneji et al. ((JP 08-191238), as cited in the IDS dated 06/22/2006.

Re claim 8, Taneji et al. discloses all the limitations of the present invention, but does not disclose further comprising an inversion circuit to which the voltage between the ground side current bypass transistor and the current limitation resistive element is input so as to invert the input voltage to control the power supply side output control transistor. However, transistor 36 is an N-type transistor. It is well known in the art to interchange the N-type transistor with an inverter in series with P-type transistor due to circuit equivalence. Therefore, it would have been obvious to one of ordinary skill in the art to interchange the N-type transistor with an inverter in series with P-type transistor, for the purpose of using equivalent circuitry for the same functionality.

Re claim 10, Taneji et al. discloses all the limitations of the present invention, but does not disclose, wherein the ground side output control transistor, the power supply side output control transistor and the ground side current bypass transistor are MOS transistors. However, it is well known in the art that BJT transistors are replaceable with MOS transistors due to MOS transistors having characteristics of better handling larger amount of current and smaller size. Therefore, it would have been obvious to one of ordinary skill in the art to exchange the BJT transistors with MOS transistors, for the purpose of decreasing size of the circuitry.

8. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taneji et al. ((JP 08-191238), as cited in the IDS dated 06/22/2006 as applied

to claims 7 and 8 above, and further in view of Applicants Admitted Prior Art (AAPA), Figure 2.

Re claim 11, Taneji et al. further discloses wherein the base current supply resistive element and the current limitation resistive element are resistors, but does not disclose the second current limitation resistive element.

Applicant's AAPA teaches in Fig. 2 the second current limitation resistive element (26), which is a resistor. Applicant further teaches a signal output circuit 102 that would be equivalent to the circuit taught in Taneji et al.

Therefore, it would have been obvious to one of ordinary skill in the art to use the circuit disclosed in Fig. 5 of Taneji et al. in 102 of Applicant's AAPA, for the purpose of using equivalent circuitry for the same functionality.

Re claims 12, 13, and 14, Taneji et al. discloses all the limitations of the present invention, but does not disclose the resistive elements, the reference voltage generation circuit, and the comparator.

Applicant's AAPA teaches in Fig. 2 the signal output circuit (102), further comprising:

resistive elements connected in series and arranged to divide the power supply voltage (23, 24);

a reference voltage generation circuit arranged to generate the reference voltage (22); and

a comparator (25) arranged to compare the voltage at a mid-point of said resistive elements connected in series (23, 24) and the reference voltage generated by said reference voltage generation circuit (Vref) so as to use the comparison output as an input signal of the signal output circuit (102), wherein the output signal of the signal output circuit is output as a power supply voltage monitoring signal (out).

Therefore, it would have been obvious to one of ordinary skill in the art to use the circuit disclosed in Fig. 5 of Taneji et al. in 102 of Applicant's AAPA, for the purpose of using equivalent circuitry for the same functionality.

Allowable Subject Matter

9. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Re claim 9, the prior art does not teach or fairly suggest a signal output circuit comprising a second current limitation resistive element connected to the output of said inversion circuit.

Response to Arguments

On pages 6-7, Applicant respectfully states, "However, contrary to the Examiner's allegations, reference numbers 35 and 36 of Taneji et al. turn ON and OFF together and do not turn ON and OFF opposite to each other as the "power supply side

output control transistor" and the "ground side output control transistor" recited in Applicant's Claim 7 do."

Examiner respectfully disagrees. 32 and 34 operates such that when 38 is low, 34 will be turned off, thereby allowing the node between 32 and 34 to be high (voltage drop of Vs across 32), while at the same time, 35 will receive the input 38, thus causing it to turn off. Similarly, when 38 is high, 34 will be turned on, thereby creating a voltage drop so that the node between 32 and 34 will output a low signal, while at the same time, 35 will receive the input 38, thus causing it to turn on. Therefore, 36 and 35 are "arranged to turn ON and OFF in opposite ways" as claimed in Claim 7.

On page 7, Applicant respectfully states, "Thus, Taneji et al. fails to teach or suggest the feature of "a power supply side output control transistor located between the base current supply resistive element and the base of the output transistor and arranged to turn ON and OFF in opposite ways as the ground side output control transistor according to the input signal" as recited in Applicant's Claim 7."

Examiner respectfully disagrees. 32 and 34 operates such that when 38 is low, 34 will be turned off, thereby allowing the node between 32 and 34 to be high (voltage drop of Vs across 32), while at the same time, 35 will receive the input 38, thus causing it to turn off. Similarly, when 38 is high, 34 will be turned on, thereby creating a voltage drop so that the node between 32 and 34 will output a low signal, while at the same time, 35 will receive the input 38, thus causing it to turn on. Therefore, 36 and 35 are "arranged to turn ON and OFF in opposite ways" as claimed in Claim 7.

On pages 7-8, Applicant respectfully states "Contrary to the Examiner's allegation and as clearly seen in Fig. 5 of Taneji et al., reference number R6 of Taneji et al. is not located between reference numbers R7 and 34 of Taneji et al. Thus, Taneji et al. fails to teach or suggest the feature of "a current limitation resistive element located between the ground side current bypass transistor and the base current supply resistive element" as recited in Applicant's Claim 7.

Further, none of the current that flows through reference number R7 of Taneji et al. flows through reference number R6 of Taneji et al., which makes it impossible for reference number R6 of Taneji et al. to limit the current from reference R7 of Taneji et al., as is required of the "current limitation resistive element" and the "base current supply resistive element" recited in Applicant's Claim 7. Thus, Taneji et al. fails to teach or suggest the feature of "a current limitation resistive element ... limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow" as recited in Applicant's Claim 7."

Examiner respectfully disagrees. R7 is connect to R6 through Vs. Therefore, R6 is connected between R7 and 34.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIANA J. CHENG whose telephone number is (571)270-1197. The examiner can normally be reached on Monday-Friday, 9 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. J. C./
Examiner, Art Unit 2816
05/01/2008